HiPINEB 2017

The 3rd IEEE International Workshop on High-Performance Interconnection Networksin the Exascale and Big-Data Era

Austin, TX, USA, 5 February 2017
http://hipineb.i3a.info/hipineb2017/

To be held in conjunction with the HPCA Conference 2017

ABSTRACT

By the year 2023, High-Performance Computing (HPC) Systems are expected to break the performance barrier of the Exaflop (10^18 FLOPS) while their power consumption is kept at current levels (or increases marginally), what is known as the Exascale challenge. In addition, more storage capacity and data-access speed is demanded to HPC clusters and datacenters to manage and store huge amounts of data produced by software applications, what is known as the Big-Data challenge. Indeed, both the Exascale and Big-Data challenges are driving the technological revolution of this decade, motivating big research and development efforts from industry and academia. In this context, the interconnection network plays an essential role in the architecture of HPC systems and datacenters, as the number of processing or storage nodes to be interconnected in these systems is very likely to grow significantly to meet the higher computing and storage demands. Besides, the capacity of the network links is expected to grow, as the roadmaps of several interconnect standards forecast. Therefore, the interconnection network should provide a high communication bandwidth and low latency, otherwise the network becoming the bottleneck of the entire system. In that regard, many design aspects are considered when it comes to improving the interconnection network performance, such as topology, routing algorithm, power consumption, reliability and fault tolerance, congestion control, programming models, control software, etc.

The main goal of the third edition of HiPINEB is to gather and discuss in a full-day event the latest and most prominent efforts and advances, both from industry and academia, in the design and development of scalable high-performance interconnection networks, especially those oriented to meet the Exascale challenge and Big-data demands.

All researchers and professionals, both from industry and academia, working in the area of interconnection networks for scalable HPC systems and Datacenters are encouraged to submit an original paper to the workshop and to attend this event.

TOPICS OF INTEREST

The list of topics covered by this workshop includes, but is not limited to, the following:

- Interconnect architectures and network technologies for high-speed, low-latency interconnects.
- Scalable network topologies, suitable for interconnecting a huge number of nodes.
- Power saving policies in the interconnect devices and network infrastructure, both at software and hardware level.
- Good practices in the configuration of the network control software.

- Network communication protocols: MPI, RDMA, MapReduce, etc.
- APIs and support for programming models.
- Routing algorithms.
- Quality of Service (QoS).
- Reliability and Fault tolerance.
- Load balancing and traffic scheduling.
- Network Virtualization.
- Congestion Management.
- Applications and Traffic characterization.
- Modeling and simulation tools.
- Performance Evaluation.
- Interfacing accelerators through the interconnect (GPUs, Xeon Phi, etc).
- Network infrastructure in distributed storage, distributed databases and Big-Data.

Furthermore, short papers in the above topics will be also taken into consideration, as long as they are based on emerging ideas, work-in-progress and early, high-impact achievements.

Note, however, that papers focused on topics that are too far from the design, development and configuration of high-performance interconnects for HPC systems and Datacenters (e.g., mobile networks, intrusion detection, peer-to-peer networks or grid/cloud computing) will be automatically considered as out of scope and rejected without review.

PAPER SUBMISSIONS

Regular and short papers must be in PDF format and should include title, authors and affiliations as well as the e-mail address of the contact author. Submitted regular manuscripts may not exceed 8 single-spaced double-column pages using 10-point size font on 8.5x11 inch pages, including figures, tables, and references. Short papers may not exceed 4 single-spaced double-column pages using 10-point size font on 8.5x11 inch pages. At least one author of the paper must be registered for the conference workshop. The conference style is based on IEEE (available at: http://www.ieee.org/conferences_events/conferences/publishing/templates.html).

HiPINEB manuscript submissions are managed by easyChair. To submit a paper, go to https://easychair.org/conferences/?conf=hipineb2017 and follow the instructions.

REVIEW PROCESS

Authors are entitled to submit original papers of high technical quality, according to the list of topics described above. Papers will be reviewed based on originality, novelty, technical strength, presentation quality, correctness and relevance to the conference scope.

WORKSHOP PROCEEDINGS

Papers will be published in the HiPINEB proceedings, edited by the IEEE CPS which will be submitted for indexing and inclusion in IEEE Xplore and CSDL.

SPECIAL ISSUE

Best papers among those selected for HiPINEB 2017 will be published in a Journal Special Issue with high impact factor. Further details will be provided soon.

IMPORTANT DATES

Submission Opens:	20 September 2016
Paper submission due:	20 November 2016
Notification of acceptance:	1 January 2017
Camera-ready papers due:	TBA
Early Registration due:	TBA
Workshop date:	5 February 2017

All deadlines are set at 11:59 p.m. anywhere on Earth (cf. http://wirelessman.org/aoe.html).

PROGRAM HIGHLIGHTS

- Keynote: TBA
- Technical sessions: Presentation of regular and short papers
- Panel: TBA

WORKSHOP ORGANIZATION

Organizers:

- Pedro Javier Garcia, University of Castilla-La Mancha, Spain
- Jesus Escudero-Sahuquillo, University of Castilla-La Mancha, Spain

Program Committee:

- TBA

Steering Committee:

- Jose Duato, Technical University of Valencia, Spain
- Francisco Jose Quiles, University of Castilla-La Mancha, Spain
- Torsten Hoefler, ETH Zurich, Switzerland
- Timothy M. Pinkston, University of Southern California, USA
- Eitan Zahavi, Mellanox, Israel

ADDITIONAL INFORMATION

For more information on HiPINEB 2017 check the website at: http://hipineb.i3a.info/hipineb2017 or, if you have any question, please contact the workshop organizers at hipineb@dsi.uclm.es